Model-based scanner tuning for process optimization

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ABSTRACT

Given the continually decreasing k1 factor and process latitude in advanced technology nodes, it is important to fully understand and control the variables that impact imaging behavior in the lithography process. In this joint work between TSMC and ASML, we use model-based simulations to characterize and predict the imaging effects of these variables and to fine-tune the scanner settings based on such information in order to achieve optimal printing results on a per-reticle basis. The scanner modeling makes use of detailed scanner characteristics as well as wafer CD measurements for accurate model construction. Simulations based on the calibrated model are subsequently used to predict the wafer impact of changes in tunable scanner parameters for all critical patterns in the product. The critical patterns can be identified beforehand, either experimentally on wafer, mask or through model simulations. A set of optimized scanner setting offsets, known as a "scanner tuning recipe" is generated to improve the imaging behavior for the critical patterns. We have demonstrated the efficacy of this methodology for multiple-use cases with selected ASML scanners and TSMC processes and will share the achieved improvements on defect reduction and yield improvements.
Keywords: scanner tuning, model-based, reticle specific optimization, manufacturing environment, low-k1 imaging

1. INTRODUCTION

Continuously shrinking technology drives the need for precise control and active tuning of the lithographic parameters for the optimization of manufacture yield and production quality. One example is the tuning of the optical parameters on one scanner such that its imaging performance on a particular production layout is matched to a specific so-called reference scanner[1 2].

In earlier work, we demonstrated that by using model-based scanner tuning in combination with full-chip analysis we were able to improve the matching performance and attain higher yield for the specific design in question[3]. In this work, we will show the application of the same scanner-tuning methodology for two new use cases, namely the correction of a marginal bridging defect and the fine-tuning of the CD-through-pitch behavior to address an IDDQ leakage problem.

Also in this work, we will show the application of the above procedure on manufacturing processes for **advanced technology node OD** and **mature technology node poly** layers; both use cases involve real production layouts. Different from the conventionally used optical proximity correction (OPC) process in which the mask layout design is modified in order to avoid defects ("hot spots") occurring in the lithographic process or changes in the layout design, the scanner tuning method can perform design-specific tuning to repair known defects or intentionally change the layout design by the required amount without having to go through the time-consuming mask-making process, meanwhile ensuring that all other patterns are picked up from full layout to change within an acceptable range.

The procedure described above for scanner tuning is referred to as LithoTuner in this work.

2. METHODOLOGY

Lithographic models are customized to serve their specific purposes. In the model-based OPC process, the lithographic models used for full-chip simulations are required to have good prediction accuracy under a fixed lithographic condition plus possible focus and exposure dose variations, also known as process window (PW). Thus, the models are calibrated

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with wafer CD data exposed under different dose and focus conditions and the calibrated model, in turn, remains accurate throughout the focus/exposure PW[4].

For scanner tuning purposes, the requirement for model calibration is illustrated in Figure 1.

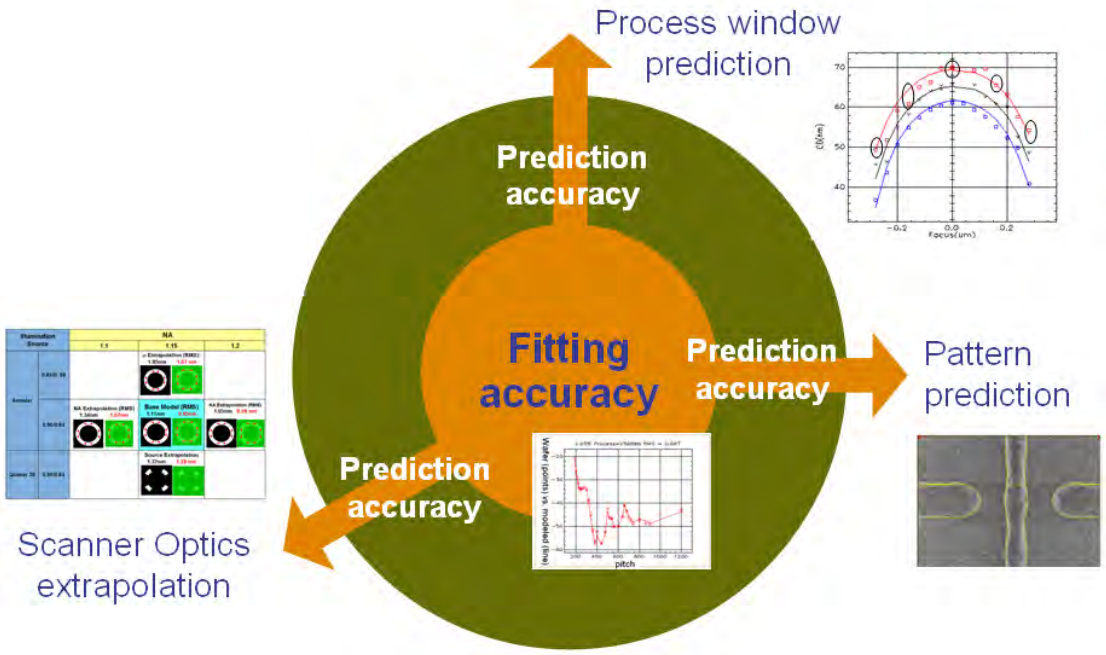

Figure 1 Models used in scanner tuning require good accuracy for process window prediction, pattern contour prediction and scanner optics extrapolation of a pattern's image prediction.

However, for scanner tuning purposes, there is an additional requirement for model accuracy beyond that for OPC models. Because changes of optical parameters of a lithographic system are used to optimize the image behavior of patterns, the models are calibrated with wafer CD data exposed under conditions with different scanner optical parameters[3].

Based on Tachyon models calibrated across a full optical parameter space, we can predict the pattern's "sensitivity" to scanner knobs. Thus, the optimization can be carried out according to a set of critical patterns selected based on the overall product performance.

For scanner optimization, we first analyze all patterns to assess whether they are at risk for creating defects such as bridging, necking and CD uniformity issues. Next, we add these at-risk patterns to the set of tuning targets for the scanner optimization. This set of tuning targets is input to an optimization module together with the lithographic model which has the required sensitivity accuracy. A set of scanner-knob changes, called the tuning recipe, is the output to achieve the tuning target in the lithographic process. This approach ensures that we do not accidentally propose a tuning recipe that turns an at-risk pattern into a real defect. In the meantime, we can also monitor changes of any patterns of interest which are not used in the optimization process under this tuning recipe. The maximum change induced by tuning on the monitored patterns can also be used as a constraint for the optimization procedure.

3. RESULTS

3.1 Test conditions

To demonstrate the efficacy of the LithoTuner methodology for design specific scanner optimization, two realistic use cases from TSMC are chosen to carry out the experiments. One bridging defect in the advanced technology node OD layer is repaired and the through-pitch behavior of the mature technology node poly layer is optimized by optical

parameter tuning of these two respective processes. In the advanced technology node OD defect repairing case, the CD impact on through pitch patterns and 2D patterns on the same layout are constrained to be within a certain range.

Besides commonly used scanner knobs such as NA, illumination source sigma settings, focus range, we also investigate the use of spokes pupicom in the illumination module of ASML scanners for this test.

3.2 Model calibration

The detailed model calibration process of the mature technology node poly layer has been reported earlier[3], and the same procedure was applied for advanced technology node OD layer model calibration. As the standard process of LithoTuner usage, the TSMC test reticle is exposed under the nominal and five different optical perturbed conditions which are predetermined to optimize the calibration procedure. Patterns used for model calibration include 1D pitch and 2D patterns and the defect pattern, as well.

For the advanced technology node OD model calibration, wafer measurement of a total of 88 patterns under these six conditions and detailed scanner metrology measurement are input into Brion's Tachyon model calibration engine. As explained before, here the model calibration mainly aims at the prediction of imaging behavior change caused by changes in optical conditions, rather than at absolute CD prediction accuracy. Mathematically it is interpreted as a set of model parameters to minimize difference between model's prediction of CD changes between perturbed and nominal optical conditions and experimentally measured CD changes. The result is shown in Figure 2. We picked one perturbed condition to illustrate the fitting results. The CD values in the figure are expressed as percentage relative to nominal feature size. Wafer CD differences and model CD differences are lined up for comparison. Those red vertical lines are for labeling patterns in different categories: anchor pattern used in the litho process, the defect, pitch and 2D patterns.

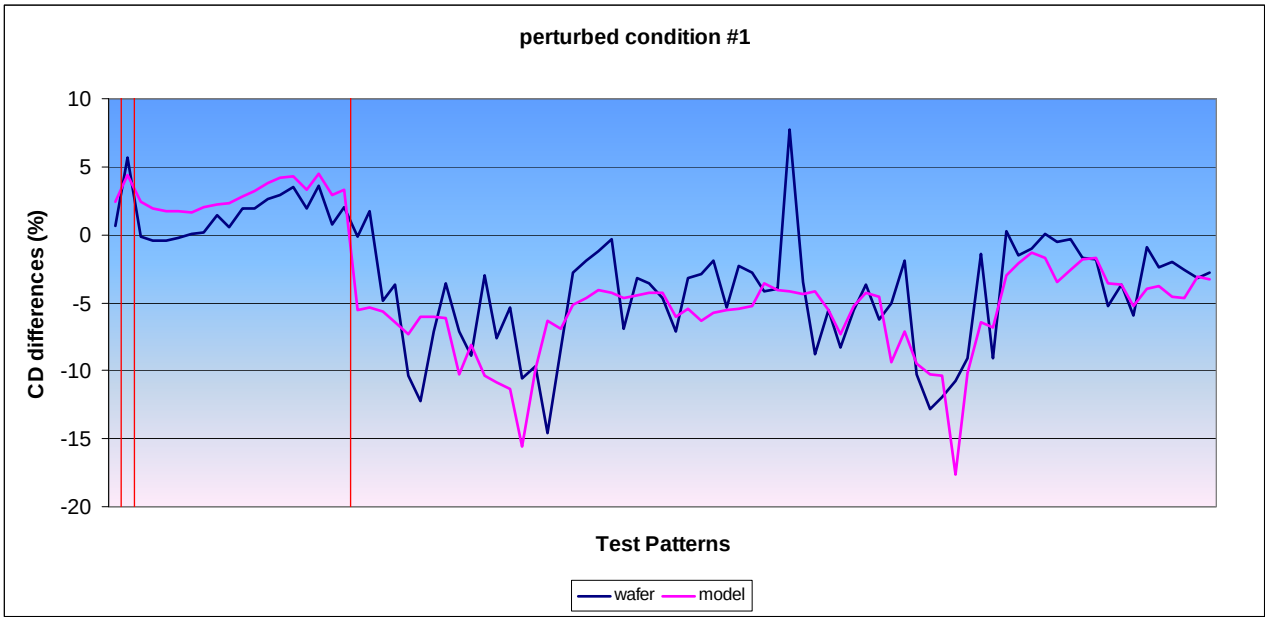

Figure 2 Wafer data versus fitted model data of CD differences between the nominal optical condition and a perturbed condition, for advanced technology node OD process. The modeling fitting procedure tries to minimize the difference between the magenta and blue curve. Different pattern categories are delimited by the red vertical lines.

Once the model is calibrated with the special cost function, it can predict patterns image behavior under a reasonable range of perturbed optical conditions retaining high accuracy.

3.3 Design Specific Scanner Optimization

For the advanced technology node OD case, the defect in question is a bridging between neighboring patterns after etching. The solution is to have the gap increased by 6% of its original target in ADI image. The OPC-based fix is to enlarge the gap on mask, which would entail both the mask making cost and a relatively long turnaround time. Alternatively, the LithoTuner method is applied to fix the problem by setting the tuning target for the defective pattern to

be 6% larger than it is with the nominal optical setting. It is also necessary to minimize the impact on the other patterns, so a certain tolerance in terms of absolute CD change was set on the 1D patterns in the tuning pattern set. The constrained optimization is carried out by LithoTuner. A tuning recipe which is a set of optical parameters offset is output by LithoTuner based on the above settings.

In the mature technology node poly layer case, it is desirable to reduce the leakage current in the product, which is translated into the lithographic metric of increasing the CDs for the isolated and semi-isolated patterns. At the same time, it is required that the dense patterns remain as close as possible to the nominal condition imaging behavior. The tuning targets are set correspondingly, with the optimization cost function defined as RMS difference of the wafer CD with respect to the tuning targets. Range-based constraints are not used in the mature technology node poly case.

3.4 Experimental validation of the tuning results

Wafer exposures are carried out using the tuning recipe computed by LithoTuner. For the advanced technology node OD case, wafer CD measurements are taken on the defect pattern and all other patterns of interest to validate the tuning, and the results in the form of CD changes as caused by tuning are shown here.

Figure 3 shows the tuning results on advanced technology node OD layer obtained with LithoTuner–based exposure recipe: both model prediction and wafer verification are plotted.

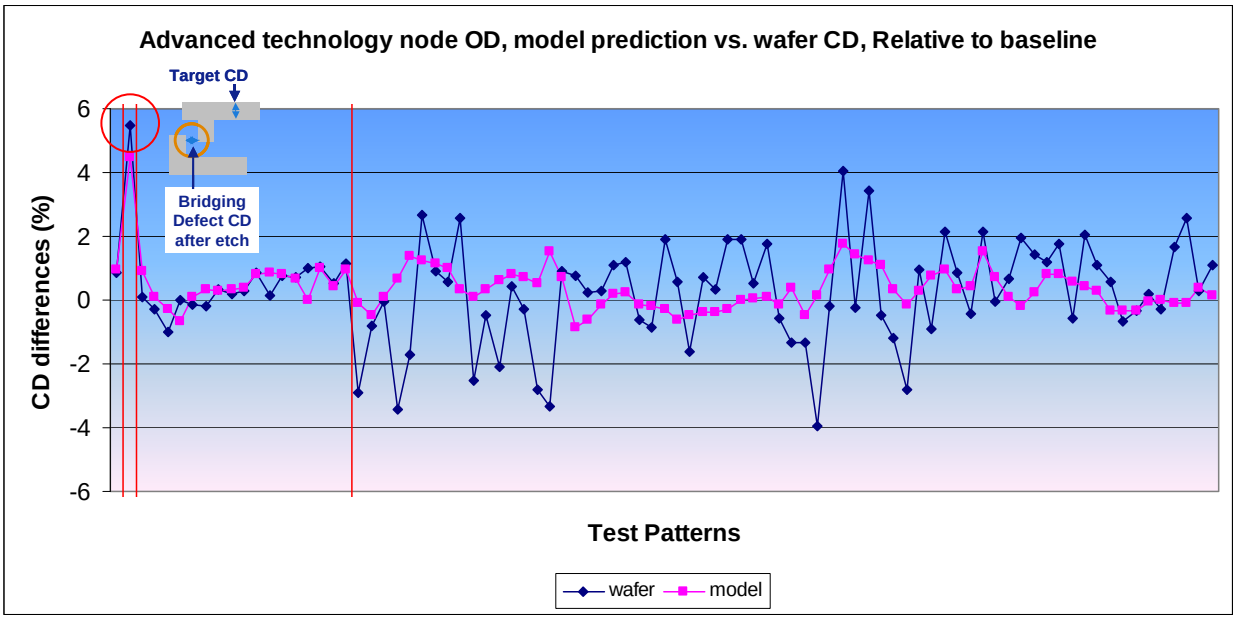

Figure 3 LithoTuner-based tuning results of repairing a bridging defect on advanced technology node OD layer. The red vertical lines here categorize patterns into anchor pattern, defective pattern, through pitch patterns and line-2D patterns.

In Figure 3 the red vertical lines categorize patterns, from left to right, into anchor pattern, defective pattern, through pitch patterns and line-end patterns. So, the defective pattern is the second pattern displayed. The tuning recipe predicts that the gap will be widened by 4.5% relative to its original target CD, and wafer exposure reveals 5.5%. In the meantime, all through pitch patterns are limited within the required range and the 2D patterns' behavior caused by tuning is predicted, as well. Most 2D line-end patterns are limited within +/-4% of their feature size.

Figure 4 shows wafer exposure validation of tuning on mature technology node poly layer compared to the output of manual tuning solution. As explained before, for dense patterns the tuning target is the nominal condition imaging behavior (blue curve) and the tuning also aims to enlarge the rest of the patterns (isolated and semi-isolated patterns). CD values are all offsets relative to the anchoring pitch.

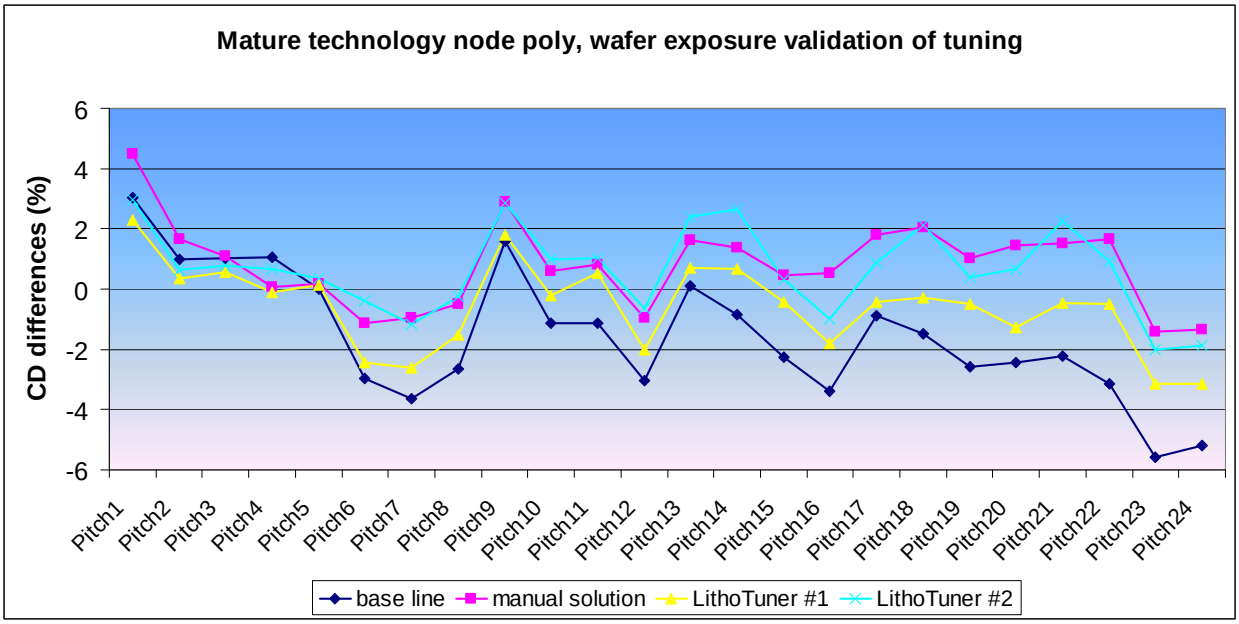

Figure 4 LithoTuner tuning results on mature technology node poly layer. Wafer exposure results from manual tuning are listed for comparison. For dense patterns, the blue curve is the tuning target and increased wafer CD is the tuning target for the rest of the patterns. Two recipes are generated by LithoTuner.

In Figure 4 there are two sets of wafer data labeled as LithoTuner #1 and #2 displayed. They are obtained from different LithoTuner tuning recipes, and their difference lies in the trade-off between the dense and the isolated patterns, i.e., by changing the relative statistical weights assigned to them in tuning. Recipe #1 has closer post-tuning results relative to base line on dense patterns, and recipe #2 ensures better tuning results on isolated and semi-isolated patterns.

In addition to statistics based on wafer measurement, wafer-acceptance-test ("WAT") results and yield analysis results of this mature technology node poly layout are also collected and compared to manual tuning solution. The WAT tests include tests on saturation current I_{sat} and threshold voltage $V_{t,}$ and the parameter values from the wafer printed under the nominal optical conditions are used as baselines. In Figure 5 are shown the RMS mismatches of the WAT parameters with respect to the reference condition results, the smaller the number, the better a process is matched to the reference condition in terms of the electrical tests. Both LithoTuner recipes lead to better matching as compared to the manual tuning solution. This is consistent with the fact that both LithoTuner solutions are predicted to produce through-pitch behaviors closer to base line compared with the manual solution result.

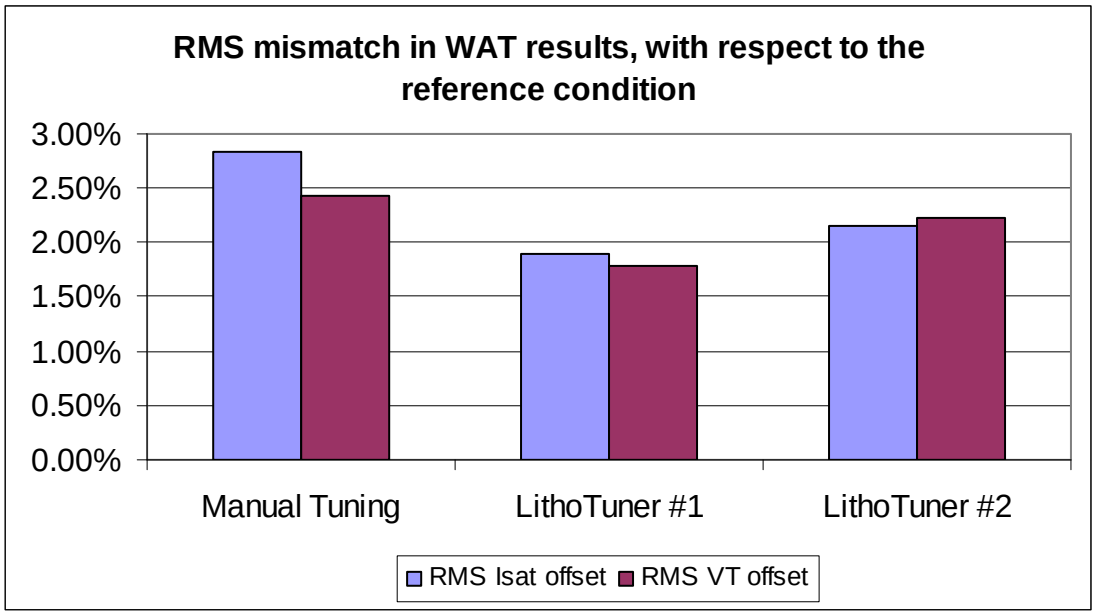

Figure 5 RMS mismatch in wafer acceptance test results, LithoTuner tuning recipes #1 and #2, as well as the manual tuning solution, are compared to the reference condition results. The smaller the RMS numbers, the better the matching in terms of electrical tests.

LithoTuner solution achieved comparable yield improvement as the manual tuning solution as well. Here it is useful to point out that, whereas the manual tuning solution required various wafer-based iterations and consumed a total time period of approximately 3 months, the LithoTuner solution was obtained in a matter of a few days. The results are shown in Figure 6. We therefore conclude that LithoTuner consistently produced tuning superior solutions in a fraction of the time.

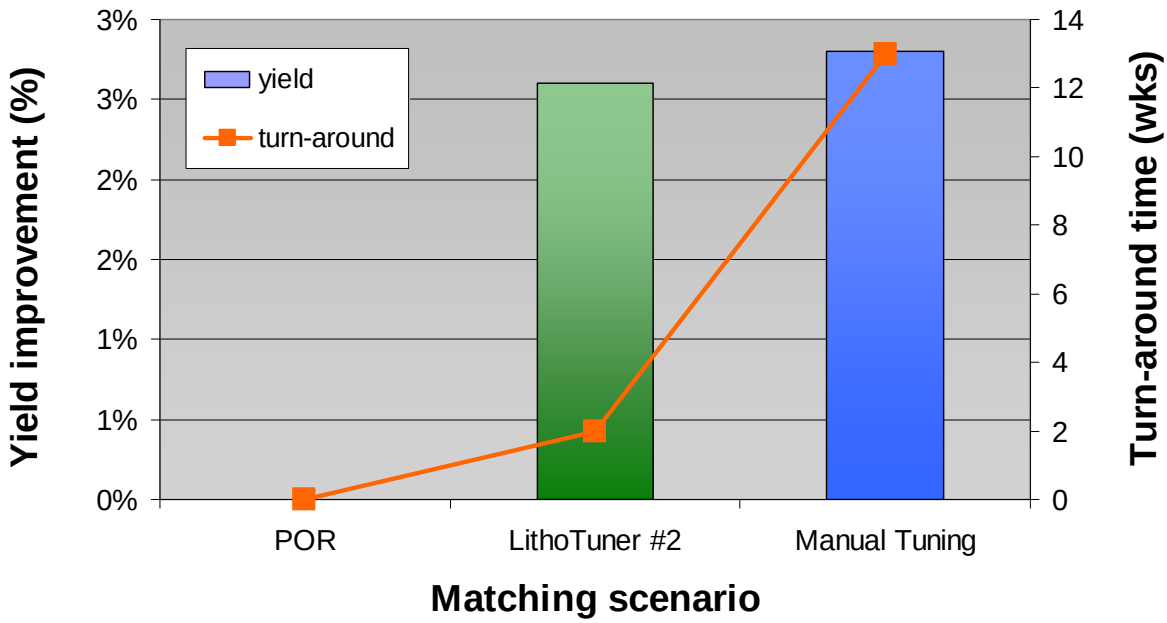

Figure 6 Yield improvement and turn-around time comparison between LithoTuner and manual tuning solutions. The LithoTuner solution achieves a similar level of yield improvement as the manual tuning solution in a fraction of the time.

The yield analysis again agrees with our model prediction that LithoTuner solution #2 produces yield improvement that is very comparable to the manual tuning solution. This is easy to understand because yield is mainly determined by isolated and semi-isolated patterns on which these two tunings have similar output.

4. CONCLUSION

In this work, we have demonstrated the efficacy of LithoTuner for design-specific scanner optimization. Two successful proof-of-concept scanner tuning experiments are reported in which either defect is fixed or yield is improved by scanner tuning. We believe the LithoTuner methodology can already resolve many practical lithography issues encountered daily in the fab and can do so very expeditiously.

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